Integrated Circuit for Battery Management Systems in ISO26262 compliant vehicles

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Abstract
Ever increasing demands on formal functional safety, redundancies and reliability in electric vehicles tend to drive manufacturing costs of battery management systems up. At the same time the market is under increasing pressure to reduce cost of control electronics to meet consumer expectations on vehicle cost price structure. One way to solve this equation is to make dedicated integrated circuits for battery management systems, specifically targeting standards for formally verifiable functional safety, such as ISO 26262. This paper will give background on the EU funded ICAB project for developing such an integrated circuit.

Keywords: Battery management system, integrated circuit, ISO26262, power line communication, active balancing

1 Introduction
With the Integrated Circuit for Advanced Battery Management (ICAB) project Lithium Balance A/S and DELTA (Danske Elektronik, Lys og Akustik) address a major market opportunity by the introduction of a new battery management system (BMS) Application Specific Integrated Circuit (ASIC) for large scale lithium-ion battery packs, targeted primarily at electromobility applications. The design is an innovative integrated circuit for performing advanced battery management, at lowered cost of production, which enables improved reliability, efficiency and safety compared with currently available BMS solutions. The project result is a cutting-edge technology which could play a significant role in the mass introduction of electric vehicles (EVs) on the market worldwide.

The ICAB ASIC increases the competitiveness of automotive manufacturers and suppliers by providing them with state-of-the-art technology which:

- Meets high quality and recent safety standards, such as the ISO26262 – Functional Safety in Road Vehicles
- Improves battery performance - extends battery life and vehicle driving range
- Supports any lithium chemistry and battery pack size
- Drives manufacturing costs down significantly by means of integrated circuit technology
- Reduces the size, cost, parasitic power consumption and weight of the battery pack
- Satisfies EV consumers’ demands and meets the requirements of the automotive industry.

2 Battery management systems – the need for innovation
Globally, the emergence of electric vehicles has become a significant trend in the automotive
industry due to the technology push from new and more powerful rechargeable batteries. Political objectives such as reducing CO2 emissions, decreasing dependency on oil and promoting energy efficiency are also important drivers of electric mobility [1]. Recently, the European Commission has published a strategy to cut most of the EU greenhouse gas emissions and transforming Europe into a competitive 'low-carbon' economy by mid-century. This would involve cuts to the EU's greenhouse emissions by 80% by 2050 (compared with 1990 levels) and intermediate cuts of 25% by 2020, 40% by 2030 and 60% by 2040 [2]. These targets will only be possible by the integration of electric mobility into our systems of transport and by the replacement of fossil fuel vehicles. In this context, governments of several countries are promoting EV market uptake by providing subsidies for the automotive industry as well as incentives for the consumers (e.g., exemptions from vehicle registration tax and rebates on the cost of EVs) [3]. The population of EVs is expected to reach 3.3 million in the EU by 2020 and more than 50 million in 2030 [4].

Nevertheless, electric vehicles are still too expensive, when compared with fossil fuel vehicles, and the procurement and replenishment of batteries are largely responsible for the high price of EVs. Additionally, consumers are reluctant to invest in EV technology because of safety concerns with respect to lithium-ion (Li-ion) batteries and also due to the limited range capabilities of EVs. Battery management systems play a key role in optimizing batteries in terms of endurance, performance and reliability, and represent up to 15% of the battery cost. Despite the great efforts that have been made to promote electric mobility, improvement of BMS technology is still a challenge. It is vital to ensure that the battery pack is operated in a safe way, that the performance is optimized in order to extend the vehicle range, and that battery life is maintained to the maximum extent possible. Moreover, the cost of production will only decrease when standardized solutions start to become available, thus allowing for economies of scale. So far, many automotive OEMs (Original Equipment Manufacturers) have built alliances and joint ventures with lithium battery manufacturers. This means that the current BMS platforms certified to automotive standards are typically tailored for one car model from a specific OEM, and therefore expensive, inflexible and not commercially available for other customers. Nevertheless, recently some major OEMs of EVs have opted to forego joint ventures and have instead sourced batteries from multiple producers given the still evolving race for development of cheaper, higher capacity and safer battery packs [5].

The development in battery technology and other EV components is a critical issue in the future market uptake of EVs [6]. There is a considerable need for versatile, reliable and cost-effective BMS platforms. It is expected that the trend in the automotive industry toward greener and more efficient cars will provide significant demand for breakthrough battery management technology in the near future. The BMS market for automotive lithium batteries is estimated to 16% of a 4,200 million euro market (approximately 6,500 million euros) by 2020, with growth continuing also in the longer term [11].

3 The ICAB solution

With the ICAB ASIC Lithium Balance A/S presents a solution that overcomes the limitations of the BMS currently in the market. The novel BMS technology is a decentralized platform consisting of a master unit connected to intelligent slave units housed in each module of the battery pack (Figure 1). The latter units will enable reliable cell monitoring, cell balancing, state of the battery evaluation and communication with the master board.

![Figure 1 – ICAB overall concept.](image)

The main innovation behind this design significantly advances beyond state of the art, and aims at reducing the high component count and overall price, through the use of ASIC technology. The solution will leverage the incorporation of premium technologies in higher volume (lower cost) products. As such, the ICAB ASIC builds on the following innovative key features:
• Universal. The IC is modular, scalable and supports any lithium chemistry in the market and any battery pack size. Additionally, the technology is prepared for the emergent battery technologies currently at R&D stage (such as lithium air batteries).

• Affordable, Lightweight & Small. Standardization and miniaturization of electronic components through the ASIC (Application Specific Integrated Circuit) technology drives the cost of manufacturing down and makes the production of the system more cost-efficient than current systems on the market. The integration of an ASIC chip in each BMS slave board will significantly minimize the size of the platform, and hence the weight.

• Safe. ICAB solution is tested according to automotive international standards and complies with state-of-the-art functional safety standards.

This next generation technology presents unique features and clear advantages in terms of cost, size and weight, performance, reliability and versatility over the existing technologies. The ICAB solution is designed for large-scale production and is non-exclusively supplied to major lithium battery manufacturers and to the automotive industry in order to generate a major technological breakthrough in the batteries and automotive industries.

4 Battery management system functions

A battery management system is any electronic device that manages a rechargeable battery pack. The BMS is required to ensure that the cells in a battery are operated within their safe and reliable operating range. The BMS monitors voltages and temperatures from the cell stack. From there, the BMS processes the inputs, making logic decisions to control the pack performance, and reporting input status and operating state through communication outputs [7]. Concisely, a battery management system turns a collection of “dumb” cells into an intelligent, safe and more efficient battery pack.

The main functions of a Battery Management System are depicted in Figure 2 and can be summarized as follows [8]:

a) Battery Monitoring: BMS monitors key operational parameters, such as voltages, currents, and temperatures, during charging and discharging of batteries. Based on these values, BMS estimates the state of the battery (e.g. state of charge and the state of health).

b) Battery protection: BMS prevents the battery from operating outside its safe operating area such as: over-current, over-voltage, over-temperature and under-temperature.

c) Battery’s performance optimization: in order to maximize battery capacity, and to prevent localized under-charging or over-charging, the BMS ensures that all cells that compose the battery are kept at the same state of charge, through balancing.

d) Communication: BMS communicates the above data to users/external devices. In electric vehicles, the battery management system interfaces with other on-board systems such as engine management, climate control, communication and safety systems, responsible for communications with the world outside the battery pack.

The ICAB ASIC supports the BMS functionality in terms of cell level monitoring of voltage and temperature.

5 Battery management structure

In high power applications, around ten to over one hundred high-capacity elementary cells are series connected to build up the required battery voltage. The overall cell string is usually segmented into modules consisting of 4 to 14 series connected
cells. Thus, the battery can be composed by three layers: namely, the elementary cell, the module and the pack [9]. Within each module the cells are connected together to complete the electrical path for current flow. Modern BMS systems for EV applications are typically distributed electronic systems. In a standard distributed topology, routing of wires to individual cells is minimized by breaking the BMS functions up into at least 2 categories, pack management unit and module management units (Figure 3).

Figure 3 – BMS structure scheme (adapted from [9])

The monitoring of the temperature and voltage of individual cells is done by a BMS “sub-module” or “slave” circuit board, which is mounted directly on each battery module stack [7], (in a normal passenger car the number would be 10-15 modules). Higher level functions such as computing state of charge, activating contactors along with aggregating the data from the sub-modules and communicating with the engine control unit are done by the BMS ‘master’ or ‘main module’. The sub-modules and main module communicate on an internal data bus such as CAN (controller area network) [7]. In an electric vehicle, the pack management unit is linked to the vehicle management system through the external CAN bus. Almost all electronic functions of the EV battery pack are controlled by the BMS, including the battery pack voltage and current monitoring, individual cell voltage measurements, cell balancing routines, state of charge calculations, cell temperature and health monitoring, which ensures overall pack safety and optimal performance, and communication with the vehicle management system [7].

The ICAB ASIC supports the battery management structure by implementing the required cell voltage and temperature monitoring functions on the slave module. The slave board either be accessed directly from the master module using a Serial Peripheral Interface (SPI) bus or via a microcontroller on the slave board (in this case typically using a CAN bus).
6 The ICAB specification process

The specification of the ICAB ASIC has been performed by Lithium Balance in close co-operation with leading automotive manufacturers in Europe and North America. The requirements has been broken down and analyzed in accordance with ISO26262 “Functional Safety – Road Vehicles”. See figure 4 for an example of requirement break-down and decomposition.

The specification process identified the following five safety goals on the item level (item in this case being defined as the energy storage system of an electric vehicle):

1. The energy storage system shall protect the operator from the hazards associated with battery fire. ASIL D.
2. The energy storage system shall protect the operator from the hazards associated with non-battery related fires inside the ESS. ASIL A.
3. The energy storage system shall protect the operator from the hazards associated with toxic fumes from the battery. ASIL A.
4. The energy storage system shall maintain the ability to deliver power during vehicle operation. ASIL C.
5. The energy storage system shall protect the operator from electrical shock. ASIL A.

Figure 4 – Requirement break-down and decomposition
7 The ICAB design process

The ASIC design process specified and implemented by DELTA for the purpose of the ICAB project includes the following key milestones and phases (figure 5):

1. Definition Phase
2. Requirement specification sign-off
3. Architectural Design Phase (high-level circuit blocks)
4. Detailed Design Phase (Analogue schematics, Digital code, mixed-signal verification)
5. Layout Phase (Place & Route, chip assembly)
6. Tape out - Engineering sample validation (Lab characterization)
7. Supply Chain Setup incl. Test Program Development
8. Manufacturing and supply
9. Production
8 ASIC verification
The ICAB ASIC design has been verified using inspection and simulation of all functional blocks of the design. The verification process was executed in parallel with the development procedure in small increments to ensure that no incorrect or faulty functionality was introduced into the design.

8.1 Design Review Procedure
The design and implementation has been verified by review with focus on the following items:
- Correct implementation of the interface toward the analogue block and the external interface (SPI)
- Correct timing of signals
- Correct usage of synchronous signals and non-synchronous signals.
- Sufficient safety mechanisms
- Functional implementation
- Correct and implementation of the test benches and test cases
- Sufficient coverage of functional test in test benches and test cases.

8.2 Block Simulation
All ASIC sub-blocks, both analogue and digital, have been fully verified by simulation. Test benches and test cases have been specified and implemented for each of the simulated sub-designs. All digital logic test benches are implemented in VHDL and include mechanisms for self-checking. Code coverage measurements for the simulations have been considered when relevant.

All analogue circuits have been Spice simulated with test cases for transient (functionality and settling), DC (functionality and operating range) and AC (stability) simulations. These test cases have been performed in worst case scenarios (temperature, supply voltage and process outcome parameters) and with Monte-Carlo setup (process parameter mismatch). Each test case is setup to enable reproducible regression test/verification simulation. Fault injection during simulation has been performed when relevant.

The generated simulation log files have been inspected and any discrepancies recorded and analysed.

8.3 System Simulation
Test bench and test cases have been specified and implemented for simulation of the system, i.e. full chip, design. All digital test benches are implemented in VHDL and implement mechanisms for self-checking.

Code coverage measurements for all simulations of the design have been performed. The goal of these measurements is a coverage metric > 98%; coverage metrics below this shall be analysed and corrective actions performed.

Simulation of test cases with fault injection has been performed. If a failure as a result of the injected fault is detected, the failure and effect shall be analysed and corrective actions taken when applicable.

Analogue system simulations are performed as Spice simulations with the same verification methodology as for the block design.

Simulation log files have been inspected. Any discrepancies are recorded and analysed.

8.4 Gate Level
This section covers the tasks involved in the verification of the gate level implementation (gate net list) of the digital design. The gate net list is the simulation model obtained through synthesis and subsequent layout of the RTL design.

8.4.1 Inspection of Implementation
The inspection of the gate net list covers the following items:
- Verify that the gate net list has been implemented as expected
- Verify that the safety structures are implemented and have not been removed during synthesis.
- Verify that the scripts used for performing synthesis and layout are correct.
- Inspect the log files from synthesis and layout

8.4.2 Static Timing Analysis
Static timing analysis has been performed on the gate net list with back-annotated timing information extracted from the layout. No timing violation results are allowed.

Timing report files and tool log files shall be inspected for correct tool behaviour.
8.4.3 Logic Equivalence Check
A logic equivalence check between the RTL design and the gate level net list has been performed.
Tool log files have been inspected for correct tool behaviour.

8.4.4 Scan Pattern Generation
Scan test patterns for production test have been generated. The fault coverage shall be above 98% for all stuck-at faults.
The generated scan test patterns were simulated using the gate-level net list with back-annotated timing information extracted from the layout.
Scan vector generation tool log files have been inspected for correct tool behaviour.
Log files from the simulations have been inspected. Successful timing annotation has been checked and timing violations analysed.

8.5 Layout
The digital layout is a placed and routed representation of the gate net list. This is done using a software tool.
The analogue layout is done manually observing the following constraints:
- Device matching
- Distribution of power and bias nets
- Noise and temperature coupling
- Parasitic capacitance
- Foundry design rules
- Latch-up prevention
- ESD tolerance

Some of the layout checks which are also covered by checks performed in later stages of the chip assembly process have been omitted.

8.5.1 Power distribution
The optimal power distribution network has been verified during the layout generation. Correct and acceptable voltage drops have been verified.

8.5.2 Layout Inspection
The digital standard cell layout block resulting from the physical implementation of the gate net list has been verified. Special focus was placed on the following items during the inspection:
- Correct and sufficient power distribution.
- Routing of the external signal connections (pins)
- Size and shape of the block shall fit the overall chip floorplan.

- Inspection of the layout tool log files to ensure correct tool behaviour.

8.6 Chip Level Verification
These verification tasks are performed on the whole chip. The whole chip is the assembly of both the analogue and the digital parts. Both simulation models and the layout data base data are involved in these checks.

8.6.1 Chip Level Simulation
Full chip simulation has been performed to verify that correct assembly of the chip. The simulation includes the following stages:
- A start-up simulation that verifies that the chip will enter a known state. This simulation shall be performed on a complete transistor level net list.
- Simulations that demonstrates the correct behaviour of key functionality. These simulations can be performed in a mixed-language setup (gate net list and transistor level).

It is mandatory that the transistor level net list is simulated because this net list forms the basis for the layout equivalence check (Layout versus Schematic) check.
Log files and waveforms from the simulation has been inspected to assess the result of the simulation and verify the correct behaviour of the simulation tool.

8.6.2 Chip-Level Design Inspection
The chip level design has been inspected with focus on the following items:
- Correct pin-out
- Correct and sufficient power connections to various power domains
- Correct implementation of the safety mechanisms

8.6.3 Design Rule Check (DRC)
Design rule checks have been performed using two independent verification tools.
Any rule violation reported by the tools has been analysed and resolved. No rule violation is accepted unless it has been waived and an explanation of the violation and consequence has been recorded.
Log files and reports have been inspected to assess the results and verify the correct behaviour of the verification tools.
8.6.4 Layout versus Schematic (LVS)
Layout equivalence with transistor net list check has been performed with two independent tools. It is a prerequisite that the full transistor net list has been verified through simulation. A complete match is required. Log files and reports have been inspected to verify to assess the results and the correct behaviour of the verification tools.

8.6.5 Antenna Check
Process antenna check has been performed using two independent tools. All rule violations reported by the tools shall be analysed and resolved. No rule violation may be accepted unless it has been waived, and an explanation of the violation and consequence has been recorded. Log files and reports shall be inspected to verify to assess the results and the correct behaviour of the verification tools.

9 ASIC characterization
The ICAB ASIC is at the time of writing being taped out on engineering wafers. These prototype units will be fully characterized by DELTA as part of their project contribution. This section specifies the expected performance characteristics of the ASIC.

Table 1: Measurement characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell voltage inputs</td>
<td>3</td>
<td>16</td>
<td>#</td>
</tr>
<tr>
<td>Temperature sensor inputs</td>
<td>0</td>
<td>16</td>
<td>#</td>
</tr>
<tr>
<td>Cell voltage range</td>
<td>1.5</td>
<td>4.5</td>
<td>V</td>
</tr>
<tr>
<td>Cell voltage total error</td>
<td>-</td>
<td>2</td>
<td>mV</td>
</tr>
<tr>
<td>Cell voltage settling time</td>
<td>-</td>
<td>1</td>
<td>mS</td>
</tr>
<tr>
<td>Output voltage</td>
<td>0</td>
<td>3.3</td>
<td>V</td>
</tr>
</tbody>
</table>

Table 2: Electrical characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (5V)</td>
<td>4.75</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Supply voltage (3.3V)</td>
<td>3.14</td>
<td>3.47</td>
<td>V</td>
</tr>
<tr>
<td>Power consumption (5V)</td>
<td>-</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>Power consumption (3.3V)</td>
<td>-</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td>Parasitic current</td>
<td>-</td>
<td>15</td>
<td>µA</td>
</tr>
</tbody>
</table>

Table 3: Environmental characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating temperature</td>
<td>-40</td>
<td>85</td>
<td>V</td>
</tr>
<tr>
<td>ESD (HBM, AEC Q100)</td>
<td>-</td>
<td>4</td>
<td>kV</td>
</tr>
</tbody>
</table>

10 Conclusion
With the successful conclusion of the ICAB project Lithium Balance A/S and DELTA will fill an important niche in the BMS market ecology with an ASIC that:
- Fully supports state-of-the-art standards and methodologies for functional safety [10].
- Is designed in collaboration with some of the most well-known automotive manufacturers in Europe and North America.
- Supports up to 16 cells on a single ASIC creating an excellent fit for all 48V systems (including but not limited to automotive applications).
- Fully supports the scalability and adaptability required by automotive manufacturers.
- Is ready to be produced at sufficient volumes to support series production of passenger cars.

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